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Call for papers

Special Issue on Network-on-Chips (NoCs)

1. Description and motivations

In the many-cores era, as the number of cores on a chip increases, communication solutions are evolving in order to support the new inter-core communication demands. It has been recognized that traditional bus-based interconnect architectures have reached their scalability limit, and are no longer adequate for deep-sub-micron (DSM) technologies. A Network-on-Chip (NoC) is generally viewed as the ultimate solution for the design of modular and scalable communication architectures, and it provides inherent support to the integration of heterogeneous cores through the standardization of the network boundary. In an NoC-based system, modules such as processor cores, memories and specialized IP blocks exchange data using an on-chip network. However, there are several issues associated with NoCs, such as increased power dissipation, area efficiency, higher network latency and reduced throughput. There is no doubt in the industry and research community that the importance of NoCs has been increasing in the multicore era and that they will continue to be the foremost field of research. The goal of this special issue will be to focus on NoC platforms that effectively address and presumably can overcome the many on-chip interconnection and communication challenges that already exist in today's chips or will likely occur in future chips.

This special issue of the Journal of Parallel and Distributed Computing (JPDC) is seeking original unpublished research articles that describe recent advances and efforts in the design and development of Network-on-Chip (NoC) architectures. Topics of interest to this special issue include, but are not limited to:

- NoC architecture (topology, routing, arbitration. . .)
- Novel interconnect links/switches/routers
- Signaling and circuit design for NoC links
- Power and energy issues
- Timing, synchronous/asynchronous communication
- NoC reliability issues
- NoC services (quality of service, security)
- Methodologies, tools, design flows and development environments for NoCs
- Modeling, simulation, and synthesis of NoCs
- Verification, debugging and testing of NoCs
- Floorplan-aware NoC architecture optimization
- Physical design of interconnects and NoCs
- 3D stacked, optical and RF on-chip/inpackage interconnects
- Emerging technologies for NoCs (Optics, CNFET, Nanowires)
- O/S and programming model support for NoCs
- Mapping of applications onto NoCs
- NoC support for CMP and MPSoCs
- NoCs for FPGAs and structured ASICs

- IP protocol support (AXI, OCP) and interoperability support
- Metrics and benchmarks for NoCs
- Multicore/many-core workload characterization and evaluation
- NoC design case studies

Deadlines

Paper Submission Date: 1 March 2010

Acceptance Notification: 1 September 2010

Final Papers: 1 October 2010

2. Submission requirements

Authors should follow the JPDC manuscript format as described in the "Information for Authors" at the end of each issue of JPDC or at <http://ees.elsevier.com/jpdc/>. Authors should submit their papers by 1 March 2010. The review decision will be communicated to the authors by 1 September 2010. The journal version will be reviewed as per the JPDC review process for special issues.

All manuscripts and any supplementary material should be submitted through the Elsevier Editorial System (EES) at <http://ees.elsevier.com/jpdc>.

Authors must select "Special Issue: Network-on-Chips (NoCs)" when they reach the "Article Type" step in the submission process. First-time users must register themselves as Author. For the latest details of the JPDC Special Issue see <http://ace.cs.ohiou.edu/~avinashk/jpdc.html>.

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