60 GHz OOK Transmitter in 32 nm DG FinFET Technology

Soumyasanta Laha, Savas Kaya, Avinash Kodi and David Matolak

School of Electrical Engineering & Computer Science, Ohio University, Athens, OH 45701, USA
Email: {sl922608, kaya}@ohio.edu

Abstract—There are several 60 GHz transceiver architectures that have been explored and reported in the past employing the On Off Keying (OOK) Modulation. All of these designs are primarily based on the conventional bulk CMOS architecture. In this paper, we propose a power efficient double gate (DG) MOSFET based OOK Transmitter in 32 nm DG FinFET technology. The proposed novel OOK modulator consists of only two DG-MOSFETs, making the circuit extremely power and area efficient. The LC oscillator can be tuned via back gate bias to vary the amplitude as well as frequency. The phase noise of the oscillator has a value of -133 dBc/Hz which is comparable to LC oscillator in conventional CMOS. The wide band power amplifier (PA) in addition to tunable characteristics also excels in other figures of merit such as gain (6-8 dB), 3-dB bandwidth (∼40 GHz) and linearity ($I_{IP3} = 18.7$ dBm) when compared to some recent works in different other technologies.

I. INTRODUCTION

Fundamental roadblocks in sustaining transistor miniaturization trends simply by reducing device dimensions or incrementally evolving building materials imply that more dramatic architectural changes are also needed. As a result, in sub-22 nm scale, MOSFETs built on Silicon on Insulator (SOI) substrates with ultra-thin channels and precisely engineered source/drain contacts will be replaced by 3D-engineered multi-gate devices [1]-[3]. Such multi-gate MOSFET architectures can efficiently control the channel from multiple sides instead of the top-side in planar bulk MOSFETs. The ability to alter channel potential by multiple (e.g. double, triple, cylindrical) gates provides a relatively easier and robust way to control the channel electrostatics, reducing the short channel effects and leakage concerns considerably. While these advantages are widely appreciated by CMOS digital circuit designers [4],[5], it is important to recognize that the ability to handle GHz modulation, and independent gate-drive mode make the multiple-gate MOSFETs an ideal choice also for analog radio frequency (RF) CMOS applications [6].

II. DG-MOSFET DEVICES

Being simpler for 3D structural optimization and relatively easier to fabricate as compared to other MOSFET structures (MIGFET, II-MOSFET, tri-gate and so on), the DG-MOSFET architecture (Inset, Fig.1) is chosen for the simulation study exploring the potential of multigate devices for RF applications. Such a structure can be built using a modified (two gates separated and independently accessed) FinFET device architecture. Although it requires additional routing for the second (back) gate connection, the functionality gained by this second independent gate bias certainly makes this complexity worthwhile, by reducing the number of transistors and introducing tunable circuits characteristics as demonstrated in this paper.

The widely available compact models for SOI-based single-gate MOSFETs can not be used for the DG-MOSFETs, for which new surface-potential based models are still being developed. Instead either physically-rigorous demanding TCAD simulations or approximate SPICE models utilizing two back-to-back MOSFETs mathematically coupled for improved accuracy may be used. Here, we employ the latter approach. We have used ASU Predictive Technology Model for 32 nm DG FinFETs [7] with Synopsys HSPICE RF simulation for the design and analysis of the DG-MOSFET OOK Transmitter. The reliability of the ASU 32 nm DG FinFET technology model is evident from the typical transfer characteristics of an n-type DG-MOSFETs with independent back-gate biasing as shown in Fig. 1. It is obvious that the front gate threshold can be tuned via the applied back-gate voltage, which is sufficient for us to confirm the tunable functionality and carry out a comparative study. This ‘dynamic’ threshold control is crucial to appreciate tunable properties of the LC oscillator and PA circuits.
III. TRANSMITTER DESIGN

The OOK transmitter consists of a voltage controlled oscillator (VCO), the OOK modulator and the power amplifier (PA), apart from the transmitting antenna as shown in Fig. 2. A matching network \((Z_0\) in Fig. 2) which maximizes the power transfer and minimizes the reflection losses precedes the 50 \(\Omega\) antenna. The entire simulations for the transmitter are performed for \(V_{DD} = 1\) V.

A. VCO & Modulator

We have chosen the differential negative resistance oscillator for our design of the VCO (Fig. 3). The DG-MOSFET based VCO can be tuned from the back gate for controlling the rms voltage \((V_{rms})\). Fig. 4 illustrates this interesting tunable feature of the DG-MOSFET VCO. Without any change in the supply, the \(V_{rms}\) can be controlled via back gate bias \((V_{bg})\), which can have application in many adaptive low power wireless systems. The bias at the back gate can also be tuned to change the oscillation frequency above a certain threshold (0.5 V for the present design in Fig. 4 inset). Although DG-MOSFET is not reputed for its noise performance, the phase noise of the 60 GHz VCO is found to be -133 dBc/Hz at 1 MHz offset (Fig. 5) which is comparable to that of bulk CMOS [8]. As expected, the phase noise is dominated by the process dependent flicker noise of slope \(\sim -30\) dB/decade. The corner frequency \(f_{cor}\) obtained is around 10 MHz.

The proposed novel DG-MOSFET based OOK Modulator consists of only two transistors making it ideal for use in ultra compact and/or low-power systems (Fig. 3). The modulator can work up to a data rate of 5 Gbps without any discernible distortion for 60 GHz carrier. The DG-MOSFET MN\(_4\) acts as the key OOK modulating device. The 60 GHz sinusoidal carrier from the VCO is fed into one of the gates of the transistor whereas the pulsed digital data is input to the other gate. The charge capacitive coupling of the two gates provided by the thin Si body determines the modulation, and therefore depends on the bias conditions of the two gates as well as device dimensions. The modulation occurs when the device operates in the saturation or in cut-off region, that is when there is either a ‘1’ or ‘0’ respectively emanating from the pulsed digital data. In other words, the modulation takes place at all instants of time. The symmetric DG-MOSFET MN\(_3\) acts as the switch and is kept at a high threshold voltage (filled symbol) for improved device electrostatics that maximizes the \(I_{ON}/I_{OFF}\) ratio. MN\(_3\) is turned on at the ‘HIGH’ state of the pulsed data and remains off at the ‘LOW’ state, maintaining the principle of OOK Modulation scheme. The modulated output is obtained at the drain of MN\(_3\). To maximize the power of the signal during transmission, the modulated output is fed to the PA.
S parameters at a V gate of all the transistors. The unique tunable feature of the degeneration inductors in this topology operate in the independent mode. The source power short distance wireless applications. All the transistors and bias voltage required, and hence ideal for use in low such as Darlington Cascode in terms of the lower supply The CS configuration has the advantage over other topology from [9] and modified to 32 nm DG-FinFET technology. (CS) three-stage class A PA (Fig. 7). The design is adapted from easy computation) [10].

B. Power Amplifier

The OOK Transmitter uses a DG-MOSFET common source (CS) three-stage class A PA (Fig. 7). The design is adapted from [9] and modified to 32 nm DG-FinFET technology. The CS configuration has the advantage over other topology such as Darlington Cascode in terms of the lower supply and bias voltage required, and hence ideal for use in low power short distance wireless applications. All the transistors in this topology operate in the independent mode. The source degeneration inductors L3, L6 and L9 along with the inter stage inductors L4 and L7 maximizes the power transfer, broadens frequency response and improves linearity [10]. The linearity is improved as the higher order distortions are eliminated by the gate inductors L4 and L7. The width of the three transistors are kept fixed at 1.0 μm. The bias voltage (Vb) is kept as well at 1 V.

Our simulation verifies the forward gain (S21) to vary from 60 to 100 GHz, maintaining a desired flatness to operate as a wide band amplifier (Fig. 8). The wide-band respond is the result of interstage source-degeneration in the present design, which can be compromised at the expense of gain and linearity. The gain changes around 12% in this frequency range, attesting to the extremity of flatness. The peak gain is observed at 8 dB. The input and output return losses (S11 & S22) are also verified from the simulation. Fig. 8 shows these S parameters at a Vbg of 0.2 V which is applied at the back gate of all the transistors. The unique tunable feature of the DG-MOSFET PA is observed in Fig. 9. Here, we can observe for Vbg between 0.2 V and 0.5 V, the forward gain varies by maximum ~ 6 dB. This happens at 60 GHz and is illustrated in the inset of the Fig. 9 that shows the gain variation with Vbg at different frequencies. The 3-dB bandwidth considered for all the cases of Vbg is 40 GHz. The unconditional stability of the amplifier is also verified measuring the rolleth stability factor, K (Fig. 10). The value of K remains > 1 in the 40 GHz operating range at all Vbg considered, indicates the PA to be unconditionally stable for this bandwidth (Also Δ < 1 from easy computation) [10].

The linearity of the PA is also observed to be competitive for low power CS configurations. The 1 dB compression point (P1dB) and the 3rd order Input Intercept Point (IIP3) are found to be 5.7 dBm and 18.7 dBm, respectively. The 13 dB difference between P1dB and IIP3 can be attributed to the scaling down of DG MOSFET to 32 nm [11]. The power added efficiency (PAE) and the fractional bandwidth (FB) of this amplifier is ~14% and 50% respectively. Table 1 compares these results with some recent works.
TABLE I
PERFORMANCE COMPARISON OF DIFFERENT WIDE BAND PAS

<table>
<thead>
<tr>
<th>Reference</th>
<th>Technology</th>
<th>Architecture</th>
<th>Frequency (GHz)</th>
<th>Gain (dB)</th>
<th>(P_{1dB}) (dBm)</th>
<th>PAE (%)</th>
<th>Fractional bandwidth (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[12]</td>
<td>0.18(\mu)m CMOS</td>
<td>Modified Darlington cascode</td>
<td>4-17</td>
<td>8-12</td>
<td>15-17</td>
<td>11-16</td>
<td>123</td>
</tr>
<tr>
<td>[13]</td>
<td>0.5(\mu)m E-mode pHEMT</td>
<td>Darlington cascode</td>
<td>0-16</td>
<td>10-13</td>
<td>7-18</td>
<td>N.A</td>
<td>200</td>
</tr>
<tr>
<td>[9]</td>
<td>90nm CMOS</td>
<td>Common Source cascade</td>
<td>52-65</td>
<td>2-5.2</td>
<td>6.4</td>
<td>7.4</td>
<td>22.2</td>
</tr>
<tr>
<td>This work</td>
<td>32nm FinFET</td>
<td>Common Source cascade</td>
<td>60-100</td>
<td>6-8 ((V_{bg})=0.2 V)</td>
<td>5.7</td>
<td>14</td>
<td>50</td>
</tr>
</tbody>
</table>

**Fig. 10.** The rollet stability factor (K) is > 1 in the operating range of 60-100 GHz verifying the PA to remain unconditionally stable in the range for all considered \(V_{bg}\)s.

**IV. DISCUSSION & CONCLUSIONS**

The impressive characteristics of a compact OOK Transmitter implemented in 32 nm DG FinFET technology has been investigated by simulation. The transmitter can be operated up to 5 Gbps data rates without degradation in performance and is ideally suited for short range and on-chip links. Our work has verified the DG-MOSFET to be a viable alternative to conventional CMOS technology in low power, highly efficient adaptive OOK Transmitter design in nano dimension. The proposed novel OOK Modulator based on only two transistors provides a power and area efficient alternative in future nano scale architectures. The VCO is ideal for use in adaptive power efficient wireless solutions in a broad range of frequencies. The PA design affirms significant improvements in bandwidth, flatness and peak gain over conventional CMOS and even III-V technologies. Moreover, dynamic gain tuning available in the proposed PA implementations cannot be efficiently achieved with conventional single-gate MOSFETs without additional area overhead. Thus, we illustrate how novel multi-gate transistors, expected to be in the market starting from 22nm-CMOS technology node, may become interesting and powerful options, especially in the independently-driven gate mode to redesign compact low-power analog systems for communication and control applications. The primary limitation of the present work is the lack of experimental verification, due to current absence of commercial DG-MOSFET processes, which may be attempted in near future.

**V. ACKNOWLEDGMENT**

This research was partially supported by the NSF Award ECCS-1129010.

**REFERENCES**